REMARKS

Entry of the foregoing amendment and reconsideration of this application is respectfully requested. By this amendment, claim 47 has been amended to rectify the numbering error pointed out by the Examiner. No new matter or additional matter for additional consideration has been entered. Claims 1-7, 28-33, and 37-51 remain in the application.

35 U.S.C. 102(b) REJECTIONS

Claims 1 thru 3, 5 thru 7, 37, 38, 42, 43, 45, and 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Kendall, U.S.P. 3,881,244. Applicant respectfully traverses this rejection.

The independent claims in this group are claims 1, 37, 45, and 49.

Claim 1 specifies "a trench defined in the dielectric region and including dielectric sidewalls, and an adjacent cavity defined at least partially by the substrate". Claim 1 further specifies "electroplated conductive material disposed within the trench". Here it will be understood by those skilled in the art that electroplated material is a specific type of material.

The Examiner has classified applicant's claimed limitation, electroplated material, as a process limitation that does not add any structural limitations. Applicant respectfully disagrees. First, the product-by-process cases cited by the Examiner, and indeed the entire product-by-process concept, applies to a claimed product, not to a component of the claimed product as is the situation in

applicant's case. Second, electroplated material is not an old or obvious product produced by a new method. Electroplated material is material produced by electroplating. There was no old electroplated material prior to electroplating.

The citation of some everyday, well known examples of terms that are analogous to the electroplated material term may help clarify this point. There are basically two types of household sugar: powdered sugar and granulated sugar. Every cook or chef in the world instantaneously knows the difference, even though they may not know how the two sugars are produced. Neither powdered sugar nor granulated sugar is an example of a product-by-process in which an old product is produced by a new method. That is to say, no one skilled in the cooking art would ever agree that sugar is an old product and the adjectives powdered and granulated do not add structural and descriptive limitations. Powdering and granulating may be processes but the products powdered sugar and granulated sugar are completely defined by their names.

Another instructive example is the term "powdered iron" used in the specification (col. 1, line 20) of Kendall (U.S.P. 3,881,244), cited by the Examiner as prior art in

the present prosecution. While powdering iron may be a process, everyone skilled in the art recognizes powdered iron. Further, there were no old powdered irons prior to the process of powdering and the descriptive title certainly does add structural limitations. Powdered iron is as different from any other form of iron as electroplated material is from any other form of material.

Another instructive example is the term "wire bonded terminal pad" used in the specification and claims of Saran (U.S.P. 6,232,662), cited by the Examiner as prior art in the present prosecution. While wire bonding may be a process, everyone skilled in the semiconductor art recognizes a wire bonded terminal pad. Further, there were no old wire bonded terminal pads prior to the process of wire bonding and the descriptive title certainly does add structural limitations. A wire bonded terminal pad is as different from any other form of terminal pad as electroplated material is from any other form of material.

Still another instructive example is the term "doped layer" used in the specification and claims of Park et al. (U.S.P. 6,274,920), cited by the Examiner as prior art in the present prosecution. While doping semiconductor material may be a process, everyone skilled in the

semiconductor art recognizes a doped layer. Further, there were no old doped layers prior to the process of doping semiconductor material and the descriptive title certainly does add structural limitations. A doped layer is as different from any other form of layer as electroplated material is from any other form of material.

While hundreds of additional examples of products defined by their unique processes could be cited, the above should be sufficient to show that those skilled in the art accept the description of hard to describe items in terms of how they are produced. In some instances the description of an item is very difficult and it is necessary for an applicant to describe the item in terms including how the item was fabricated (see for example *Ex parte Pantzer and Feier*, 176 USPQ 141 (Bd. App. 1972)).

In the present application, it is a well known fact that material deposited by electroplating is different than, for example, material deposited by sputtering or any of the various well-known chemical depositions used in the semiconductor art. Unfortunately, providing a name that differentiates the material deposited by electroplating from the other materials is very difficult. However, entitling the material "electroplated material" accurately and easily

identifies the material to any person of ordinary skill in the semiconductor art. Just as the titles powdered sugar and granulated sugar completely differentiate the two sugars for those skilled in the cooking art, so too does the title "electroplated material" differentiate the subject material from sputtered or chemically deposited material for those skilled in the semiconductor art. Thus, anyone skilled in the art will immediately understand that the electroplated conductive material disposed within the trench in the present invention is substantially different than anything disclosed by Kendall. The term "electroplated material" does inherently include structural limitations.

Claim 1 further specifies "a trench defined in the dielectric region and including dielectric sidewalls" and an inductance with "the sides of the inductance being bounded by the dielectric sidewalls and the cavity being adjacent the bottom." It is clear from the claim language that the dielectric sidewalls are part of the trench. It is also clear from the language that the sides of the inductance are bounded by the dielectric sidewalls. "All words in a claim must be considered in judging patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494. 496 (CCPA 1970).

Referring to FIG. 15, or any of the other drawings of Kendall, it can easily be seen that Kendall's inductance includes studs 9 and metal interconnects 17, none of which are even close to a trench sidewall. Clearly, anything in Kendall that could be interpreted as a trench with dielectric sidewalls does not bound his inductance, as required by applicant's claim. Thus, it is clear that nothing in Kendall's device or teaching is in any way similar to the present invention as now stated in claim 1. Therefore, Kendall does not anticipate the invention in independent claim 1 and dependent claims 2 thru 3 and 5 thru 7. Further, since Kendall does not teach any structure or concept that is even remotely similar to the structure of claim 1, applicant believes that claims 1 thru 3 and 5 thru 7 are now in condition for allowance.

Claim 37 specifies "a trench formed in the dielectric region and including side-walls defined by low dielectric material". Claim 37 further specifies "high conductivity electroplated material in the trench". In accordance with the arguments set forth above, Kendall does not disclose electroplated material in a trench "defining at least a portion of a passive electronic component." Claims 38, 42, and 43 are dependent upon claim 37 and are more limiting. Since Kendall does not teach any structure or concept that

is even remotely similar to the structure of claim 37, applicant believes that independent claims 37 and dependent claims 38, 42, and 43 are now in condition for allowance.

Claim 38 is dependent on claim 37 and specifies "the low dielectric constant material includes dielectric material defining an array of cavities therein, the dielectric material having a first dielectric constant and the cavities providing a second dielectric constant lower than the first dielectric constant to form an effective dielectric constant lower than the first dielectric constant." Since Kendall clearly does not have even one cavity in his structure he could not possibly anticipate "an array of cavities".

Claim 45 includes the limitations "high conductivity material in the trench and defining at least a portion of an inductive component" and "a sealed cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity material in the trench." Kendall does not disclose a sealed cavity of any shape or form. Certainly, Kendall does not disclose a sealed cavity in communication with a lower portion of the high conductivity material in the trench.

Claim 49 claims an intermediate component that includes the limitations "a trench formed in the dielectric region and including side-walls of low dielectric constant material and a bottom defined by the low resistivity, semiconductor substrate". Note that in all of the figures of Kendall anything that might be considered a trench including side-walls of low dielectric constant material and with a bottom defined by a low-resistivity, semiconductor substrate has its surface coated with oxide layer 7 for electrical isolation purposes. Thus, an exterior surface of the bottom could not serve as an electroplating contact for electroplating in the trench.

It is clear from the above discussion that Kendall is substantially different than the structures claimed by applicant in claims 1 thru 3, 5 thru 7, 37, 38, 42, 43, 45, and 49. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 2 USPQ2d 1051, 1053, (Fed. Cir. 1987). Also, "All words in a claim must be considered in judging patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494. 496 (CCPA 1970). Since each and every element of the above claims is not found in Kendall, it is clear that

the claims are not anticipated by Kendall. Therefore, applicant believes that claims 1 thru 3, 5 thru 7, 37, 38, 42, 43, 45, and 49 are now in condition for allowance.

35 U.S.C. 103(a) REJECTIONS

Claims 4, 41, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kendall as applied to claims 1 thru 3, 5 thru 7, 37, 38, 42, 43, 45, and 49 above, and further in view of Matsuzaki, JPO 06-120036. Applicant respectfully traverses this rejection.

Claim 4 is dependent on independent claim 1, claim 41 is dependent on independent claim 37, and claim 51 is dependent on independent claim 49. Each of the dependent claims 4, 41, and 51 specify "the high conductivity material includes copper". For all of the reasons stated above, the structure and teaching of Kendall is not similar to applicant's structure as claimed in claims 1, 37, and 49. Applicant does not believe that the addition of copper, as suggested by Matsuzaki, will overcome the deficiencies of Kendall's teaching, as described above. In fact, inductances of the type disclosed by Matsuzaki are the low quality factor (Q) prior art devices specifically mentioned by applicant in his Background of the Invention, pages 1 and 2 of the present specification. Therefore, applicant believes that claims 4, 41, and 51 are not obvious in view of any proper combination of Kendall and Matsuzaki.

Claims 28 thru 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki, JPO 06-120036 in view of Kendall, U.S.P. 3,881,244. Applicant respectfully traverses this rejection.

Claim 28 is the only independent claim in this group and it specifically claims "a low resistivity semiconductor substrate having a dielectric region formed therein with a cavity adjacent the dielectric region". Claim 28 further specifies "a first inductor of electroplated conductive material formed within a trench defined by the dielectric region" and "a bottom of the inductor being positioned adjacent the cavity".

A "cavity" is defined by Webster's New Universal Unabridged Dictionary, copyrighted 1989, as "1. any hollow place; hollow". Applicant, in compliance with standard Patent Law practices, has accepted this meaning. For example, cavity 76, which is a hollow, is positioned so that conductor 47 (which is a portion of inductor 50) is adjacent to it (see for example applicant's FIG. 10).

The Examiner admits that Matsuzaki does not disclose a cavity. That is correct. However, the Examiner alleges that Kendall discloses a cavity 25 in his FIG. 15.

Applicant respectfully disagrees. Referring to Kendall's disclosure, column 7, lines 28 through 38, Kendall clearly discloses

> Shown in FIG, 15 is one embodiment of an integrated circuit having a solid state inductor. The integrated circuit of FIG. 15 is depicted as a dielectrically isolated structure having dielectric isolation regions 25.
>
> Isolation regions 25 comprise layers 25' and region 25''. Utilizing techniques well-known in the art to form the isolation regions, layers 25' typically are comprised of silicon dioxide and regions 25'' are comprised of any suitable material, such as polycrystalline silicon, as described in the above-referenced copending patent application.

Clearly, Kendall does not even remotely suggest that isolation region 25 could include a cavity. Isolation region 25 is completely filled, not only in patent '244 but apparently in the copending application. Further, applicant specifically traverses the judicial notice taken by the Examiner that Kendall's isolation region could include a cavity.

Since neither Matsuzaki nor Kendall disclose a cavity nor a bottom of the inductor being positioned adjacent the cavity, it is clear that they could not possibly, alone or in any proper combination, render claims 28 thru 33 obvious. Therefore, applicant believes that claims 28 thru 33 are now in condition for allowance.

Claims 39, 40, 47, 48, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kendall, U.S.P. 3,881,244. Applicant respectfully traverses this rejection.

Claim 38 is dependent on claim 37 and specifies "the low dielectric constant material includes dielectric material defining an array of cavities therein, the dielectric material having a first dielectric constant and the cavities providing a second dielectric constant lower than the first dielectric constant to form an effective dielectric constant lower than the first dielectric constant." Kendall has neither a single cavity in his structure nor an array of cavities. Claim 39 is dependent on claim 38 and specifies a certain effective dielectric constant lower than the dielectric constant of the dielectric material forming the array of cavities. Claim 40 is dependent on claim 39 and more specific. Since Kendall discloses no cavities, it is clear that he cannot render either of claims 39 or 40 obvious. Similar arguments apply to claims 47, 48, and 50. As to the nature of the dielectric constant, page 9, center paragraph of applicant's specification should be consulted. Note that virtually all prior art devices are isolated in silicon dioxide (see Kendall, column 7, lines 28-39).

Claims 44 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kendall, U.S.P. 3,881,244 as applied to claims 1 thru 3, 5 thru 7, 37, 38, 42, 43, 45, and 49 above, and further in view of Farooq et al. U.S.P. 6,574,859. Applicant respectfully traverses this rejection.

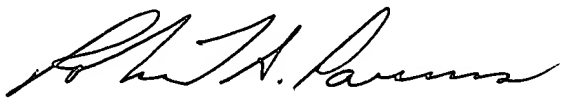
Claim 44 specifies "the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity." Claim 46 specifies "the sealed cavity is sealed by a die attach pad with a pedestal formed on a surface thereof, the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity." Kendall does not disclose a cavity and, therefore, could not suggest a pedestal positioned to seal the cavity. Clearly, nothing in Farooq et al. even remotely suggests a cavity and a pedestal positioned to seal the cavity. Thus, applicant believes that claims 44 and 46 are allowable over any proper combination of Kendall and Farooq et al.

SUMMARY

Since none of the applied references, individually or in any proper combination, disclose an integrated circuit similar to applicant's claimed structure and since none of the applied references can achieve the functions of the present invention, applicant believes that claims 1-7, 28-33, and 37-51, all of the claims presently in the application, are now in condition for allowance.

Should there be any questions or remaining issues regarding the foregoing, Examiner is cordially invited to telephone the undersigned attorney for a speedy resolution.

Respectfully requested,



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